EE / CPRE / SE 491 - sdmay20-38
iFPGA - Intermittent Intelligent FPGA Platform
Week 6 Report

9/30/19 - 10/4/19
Client: Henry Duwe
Faculty Advisor: Henry Duwe

Team Members:

Jake Tener - Team member, SW focus
Jake Meiss - Team member, HW focus
Andrew Vogler - Team member
Zixuan Guo - Team member
Justin Sung - Team member

Weekly Summary

The objective this week was to start searching for potential FPGAs and hardware components that will be integrated. Create and refine a high level block diagram of the entire system, along with researching the details associated with each component.

Past Week Accomplishments

- Component/IP Block Research - Justin Sung, Zixuan Guo, Jake Tener
    - Investigated necessary IP blocks that should be incorporated to ensure successful component integration and usage.
    - Rough block diagram of how the IP blocks should be connected
    - Market survey of microphone and transceiver components satisfying the requirements of the project (low power, relatively inexpensive, etc.)

- FPGA Market Survey Comparison - Andrew Vogler, Jake Tener
    - Researched many potential FPGAs based on criteria such as static power, dynamic power, LUTs, etc. with emphasis on low power.
    - Analyzed simulated power usage and processing power of potential FPGAs
        - IGLOO NANO was determined to be the most promising candidate

- RF Harvester/Components Research - Jake Meiss
    - Investigated the physical structures of hardware components associated with RF harvesting, capacitors, and voltage boosters, etc.
    - Researched methods of supplying required power to FPGA and designed the block diagram for the hardware components.

Pending Issues

- Scope of the project may be too big, advised to focus on a single step in the sound recognition pipeline. - Everyone

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Jake Tener	Component/IP Block Research and Design FPGA Market Survey Comparison	9	44
Jake Meiss	RF Harvester/Components Research	8	43
Andrew Vogler	FPGA Market Survey Comparison	8	43
Zixuan Guo	Component/IP Block Research and Design	8	43
Justin Sung	Component/IP Block Research and Design	8	43

Plans for Coming Week

- Synthesize the computational demands of the software and assess whether it is feasible on our FPGA platform.
- Figure out the exact numbers of how much power we can harvest from the RF source, capacitor attributes, and overall capacitor array attributes that pertain to powering the FPGA and its components.
- Synthesize some benchmark hardware on the FPGA and analyze the power requirements and computational power via adders(LUT's, etc.).
- Decide on a specific processing step in the sound recognition pipeline to tackle instead of multiple steps, too complicated as advised from Duwe.